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| **Nama** | Edgrant Henderson Suryajaya | **Kode Asisten** | ………………………… |
| **NPM** | 2206025016 | **Jenis Tugas** | TP |

1. Nomor satu

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016 is

    port (

        a, b        : IN std\_logic\_vector (7 downto 0);

        alu\_control : IN std\_logic\_vector (2 downto 0);

        alu\_result  : OUT std\_logic\_vector (7 downto 0);

        zeroflag    : OUT std\_logic

    );

end entity TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016;

architecture rtl of *TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016* is

    signal aNum, bNum, result : signed (7 downto 0);

begin

    aNum <= signed(a);

    bNum <= signed(b);

    process(aNum, bNum, alu\_control)

    begin

        case alu\_control is

            when "000" => result <= aNum + bNum;

            when "001" => result <= aNum - bNum;

            when "010" => result <= aNum and bNum;

            when "011" => result <= aNum or bNum;

            when "100" => result <= aNum xor bNum;

            when "101" => result <= -aNum;

            when "110" => result <= aNum + 1;

            when "111" => result <= aNum - 1;

            when others => result <= "00000000";

        end case;

    end process;

    zeroflag <= '1' when result = "00000000" else '0';

    alu\_result <= std\_logic\_vector(result);

end architecture rtl;

1. Nomor dua

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016\_2 is

    port (

        clk, reset      : IN std\_logic;

        reg\_write\_en    : IN std\_logic := '0';

        reg\_write\_dest  : IN std\_logic\_vector (1 downto 0) := (others => '0');

        reg\_write\_data  : IN std\_logic\_vector (7 downto 0) := (others => '0');

        reg\_read\_addrA  : IN std\_logic\_vector (1 downto 0) := (others => '0');

        reg\_read\_addrB  : IN std\_logic\_vector (1 downto 0) := (others => '0');

        reg\_read\_dataA  : OUT std\_logic\_vector (7 downto 0);

        reg\_read\_dataB  : OUT std\_logic\_vector (7 downto 0)

    );

end entity TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016\_2;

architecture rtl of *TP\_PSD5\_EdgrantHendersonSuryajaya\_2206025016\_2* is

    type RegisterArray is array (0 to 3) of std\_logic\_vector (7 downto 0);

    signal registers: RegisterArray := (others => (others => '0'));

begin

    TP\_B: process(clk, reset)

    begin

        if reset = '1' then

            registers <= (others => (others => '0'));

        elsif rising\_edge(clk) then

            if reg\_write\_en = '1' then

                registers(to\_integer(unsigned(reg\_write\_dest))) <= reg\_write\_data;

            end if;

        end if;

    end process TP\_B;

    TP\_C: process(clk)

    begin

        if rising\_edge(clk) then

            reg\_read\_dataA <= registers(to\_integer(unsigned(reg\_read\_addrA)));

            reg\_read\_dataB <= registers(to\_integer(unsigned(reg\_read\_addrB)));

        end if;

    end process TP\_C;

end architecture rtl;